DYLAN LEIFER-IVES

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EDUCATION

M.S. Computer Science June 2027

*California Polytechnic State University, SLO | **GPA: 4.0** | Advisor: Stephen Beard | Thesis: Energy-Aware Compiler Optimization via E-Graphs for GPU Kernels*

B.S. Computer Engineering, Cum Laude June 2025

*California Polytechnic State University, SLO | **GPA: 3.5** | Coursework: **Compiler Design, Operating Systems, Computer Architecture**, Systems Programming, FPGA Design, Embedded Systems*

TECHNICAL SKILLS

Languages: C/C++ · Zig · Python · SystemVerilog · x86-64 & ArmV8 Assembly
Tools: GDB · QEMU · CMake · Vivado · LLVM · MLIR · Git · Agile / TDD

EXPERIENCE

Firmware Engineering Intern June – Sept 2024

Fluke Corporation · Everett, WA

- Built a **source-to-source transcompiler** (Perl → Python) automating full migration of a legacy HIL scripting system used by ~**30 engineers** with zero manual intervention
- Designed a **CI/CD pipeline** (GitHub Actions → Zephyr RTOS → real hardware) running firmware regression tests on **every PR**, saving **2.5 hrs/day** of manual testing
- Conducted ~**20 stakeholder interviews** to design a generalized HIL automation framework; delivered ~**100 pages** of formal design documentation

Electrical Engineering Intern June – Sept 2022

Glumac (MEP Consulting)

- Designed electrical layouts for commercial projects including **Alcatraz Island** and microgrid systems in Revit and AutoCAD per California **Title 24** energy codes
- Prepared load calculations, panel schedules, and construction documentation in coordination with mechanical and plumbing engineering teams

PROJECTS

Minilang Optimizing Compiler https://github.com/probably-neb/minipp

- **Led** team of 3 to deliver full compiler in Zig (30k LOC, 170+ tests, shipped 1 week early): Pratt parser, typed IR/SSA, ArmV8 + LLVM backends.
- Implemented multi-pass optimizer: **constant propagation**, **dead code elimination**, and **loop optimizations**
- Built SSA pipeline with dominance/Cytron phi-placement and liveness-driven linear-scan allocation

Thad-OS: x86-64 Operating System Kernel in Zig https://github.com/dleiferives/thad-os

- Wrote a **higher-half x86-64 OS in Zig** (∼16,500 LOC) that boots on bare metal and runs real **Ring-3 user programs**
- Engineered **virtual memory** with demand paging, **copy-on-write fork**, and per-process address-space isolation
- Implemented a full **filesystem stack** (ext2, VFS, per-thread FD tables) and an **ELF64 loader** that executes arbitrary user binaries

M.S. Thesis: Energy-Aware Compiler Optimization via E-Graphs for GPU Kernels

- Designing an **equality saturation** framework targeting **Triton GPU kernels** at **TTIR / MLIR** level; **e-graph** representation eliminates phase-ordering to extract minimum-energy program variants
- Built an **out-of-tree MLIR pass plugin** (C++ / CMake) integrating into Triton's compilation pipeline; C++ ↔ Python bridge applies **egglog** rewrites with verified kernel correctness